Express Mail Label No. EL446775025US

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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.119.1.1
Total Pages in this Submission

JC688 U.S. PTO 09/08/99

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

JC617 U.S. PTO 09/392034 09/08/99

and invented by:

Fernando Gonzalez, David Chapek and Randhir P.S. Thakur

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☒ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: 08/985,588

Which is a:

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: 08/823,609

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: ______

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 9 pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☒ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. 11675.119.1.1
	Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   - a. ☒ Formal Number of Sheets 9
   - b. ☐ Informal Number of Sheets
4. ☒ Oath or Declaration
   - a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   - b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   - c. ☒ With Power of Attorney ☐ Without Power of Attorney
   - d. ☐ DELETION OF INVENTOR(S)
     Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   - a. ☐ Paper Copy
   - b. ☐ Computer Readable Copy *(identical to computer copy)*
   - c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
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11675.119.1.1
Total Pages in this Submission

09/08/99

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below)*:

Fee Calculation and Transmittal

CLAIMS AS FILED					
For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	43	- 20 =	23	x $18.00	$414.00
Indep. Claims	14	- 3 =	11	x $78.00	$858.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$760.00
OTHER FEE *(specify purpose)*					$0.00
				TOTAL FILING FEE	$2,032.00

☒ A check in the amount of **$2,032.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No **23-3178** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
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- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: **Sept. 7th, 1999**

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P01ULRG/REV04

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Gonzalez, et al.**			Docket No. **11675.119.1.1**
Serial No. **Not yet assigned**	Filing Date **September 8, 1999**	Examiner **Not yet assigned**	Group Art Unit **Not yet assigned**

Invention:

METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

JC617 U.S. PTO
09/392034
09/08/99

I hereby certify that this **Continuation Patent Application and related documents**
(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

Sept. 8th, 1999
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Note: Each paper must have its own certificate of mailing.

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APPLICATION INFORMATION

Title Line One:: METHOD FOR FORMING A SELF-ALIGNED ISOLAT
Title Line Two:: ION TRENCH
Total Drawing Sheets:: 9
Formal Drawings?:: Yes
Application Type:: Continuation
Docket Number:: 11675.119.1.
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Registration Number One:: 34521

CONTINUITY INFORMATION

This application is a:: CONTINUATION OF
> Application One:: 08/985,588
Filing Date:: 12-05-1997

Which is a::DIVISION OF
>> Application Two:: 08/823,609
Filing Date:: 03-25-1997

Source:: PrintEFS Version 1.0.1

Express Mailing Label No.

PATENT APPLICATION
Docket No. 11675.119.1.1

UNITED STATES PATENT APPLICATION

of

FERNANDO GONZALEZ

DAVID CHAPEK

and

RANDHIR P. S. THAKUR

for

METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

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This is a continuation of U.S. Patent Application Serial No. 08/985,588, filed on December 5, 1997, which is a divisional patent application of U.S. Patent Application Serial Number 08/823,609, filed on March 25, 1997, both of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. The Field of the Invention

The present invention relates to forming an isolation trench in a semiconductor device. In particular, the present invention relates to a method of forming an isolation trench in an etching process for a semiconductor device that combines a spacer etch with a trench etch.

2. The Relevant Technology

An isolation trench is used in an active area associated with a microelectronic device on a semiconductor substrate or on a substrate assembly. Isolation trenches allow microelectronics devices to be placed increasingly closer to each other without causing detrimental electronic interaction such as unwanted capacitance build-up and cross-talk. In the context of this document, the term semiconductive substrate is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above. The term substrate assembly is intended herein to mean a substrate having one or more layers or structures formed thereon. As such, the substrate assembly may be, by way of example and

not by way of limitation, a doped silicon semiconductor substrate typical of a semiconductor wafer.

The ever-present pressure upon the microelectronics industry to shrink electronic devices and to crowd a higher number of electronic devices onto a single die, called miniaturization, has required the use of such structures as isolation trenches.

In the prior state of the art, an etching process of fill material within an isolation trench has been problematic. As seen in Figure 1, a semiconductor substrate 12 has an isolation trench substantially filled up with an isolation material 48. A pad oxide 14 is situated on the active area of semiconductor substrate 12. Isolation material 48 exhibits a non-planarity at the top surface thereof between corners 62, particularly as is seen at reference numeral 46 in Figure 1. The non-planarity of the top surface of isolation material 48 is due to dissimilarity of etch rates between isolation material 48 and pad oxide 14, particularly at corners 62 of the active area of semiconductor substrate 12.

An active area may be formed within semiconductor substrate 12 immediately beneath pad 14, and adjacent isolation material 48. A problem that is inherent in such non-planarity of fill material within an isolation trench is that corners 62 may leave the active area of semiconductor substrate 12 exposed. As such, isolation material 48 will not prevent layers formed thereon from contacting the active area of semiconductor substrate 12 at corners 62. Contact of this sort is detrimental in that it causes charge and current leakage. Isolation material 48 is also unable to prevent unwanted thermal oxide encroachment through corners 62 into the active area of semiconductor substrate 12.

What is needed is a method of forming an isolation trench, where subsequent etching of fill material within the isolation trench of such method prevents overlying layers from having contact with an adjacent active area, and prevents unwanted thermal oxide encroachment into the active area. What is also needed is a method of forming an isolation trench wherein etching or planarizing such as by chemical mechanical planarization (CMP)

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of isolation trench materials is accomplished without forming a recess at the intersection of the fill material in the isolation trench and the material of the active area within the semiconductor substrate.

SUMMARY OF THE INVENTION

The present invention relates to a method for forming an isolation trench structure on a semiconductor substrate. The inventive method forms and fills the isolation trench without causing deleterious topographical depressions in the upper surface of the fill material in the isolation trench, while substantially preventing contact between layers overlying the fill material of the isolation trench and the active area of the semiconductor substrate. By avoiding such deleterious topographical depressions and the exposure of the active area, detrimental charge and current leakage is minimized.

The inventive method of forming an isolation trench comprises forming a pad oxide upon a semiconductor substrate and depositing a first dielectric layer thereupon. By way of non-limiting example, the first dielectric layer is a nitride layer. The first dielectric layer is patterned and etched with a mask to expose a portion of the pad oxide layer and to protect an active area in the semiconductor substrate that remains covered with the first dielectric layer. A second dielectric layer is formed substantially conformably over the pad oxide layer and the remaining portions of the first dielectric layer.

A spacer etch is used to form a spacer from the second dielectric layer. The spacer electrically insulates the first dielectric layer. An isolation trench etch follows the spacer etch and creates within the semiconductor substrate an isolation trench that is defined by surfaces in the semiconductor substrate. The spacer formed by the spacer etch facilitates self-alignment of the isolation trench formed by the isolation trench etch. The isolation trench etch can be carried out with the same etch recipe as the spacer etch, or it can be carried out with an etch recipe that is selective to the spacer. Once the isolation trench is formed, an insulation liner on the inside surface of the isolation trench can be optionally formed, either by deposition or by thermal oxidation.

A third dielectric layer is formed substantially conformably over the spacer and the first dielectric layer so as to substantially fill the isolation trench. Topographical reduction

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of the third dielectric layer follows, preferably so as to planarize the third dielectric layer for example by chemical mechanical planarizing (CMP), by dry etchback, or by a combination thereof.

The topographical reduction of the third dielectric layer may also be carried out as a single etchback step that sequentially removes superficial portions of the third dielectric layer that extend out of the isolation trench. The single etchback also removes portions of the remaining spacer, and removes substantially all of the remaining portions of the first dielectric layer. Preferably, the single etchback will use an etch recipe that is more selective to the third dielectric layer and the spacer than to the remaining portions of the first dielectric layer. The single etchback uses an etch recipe having a selectivity that will preferably leave a raised portion of the third dielectric layer extending above the isolation trench while removing substantially all remaining portions of the first dielectric layer. The resulting structure can be described as having the shape of a nail as viewed in a direction that is substantially orthogonal to the cross section of a word line in association therewith.

Several other processing steps are optional in the inventive method. One such optional processing step is the deposition of a polysilicon layer upon the pad oxide layer to act as an etch stop or planarization marker. Another optional processing step includes clearing the spacer following the isolation trench etch. An additional optional processing step includes implanting doping ions at the bottom of the isolation trench to form a doped trench bottom. When a CMOS device is being fabricated, the ion implantation process may require a partial masking of the semiconductor substrate so as to properly dope selected portions of the semiconductor substrate.

These and other features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

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BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 illustrates the prior art problem of an uneven etch of an isolation trench that results in exposing portions of an active area and unwanted thermal oxide encroachment into the active area.

Figure 2A is an elevational cross-section view of a semiconductor substrate, wherein a pad oxide and a nitride layer have been deposited upon the semiconductor substrate.

Figure 2B is an elevational cross-section view of a semiconductor substrate having thereon a polysilicon layer that has been deposited upon a pad oxide, and a nitride layer that has been deposited upon the polysilicon layer.

Figure 3A illustrates further processing of the structure depicted in Figure 2A, wherein a mask has been patterned and the nitride layer has been etched down to the pad oxide layer to form a nitride island over future or current active areas in the substrate that are to be protected.

Figure 3B illustrates further processing of the structure depicted in Figure 2B, wherein a mask has been patterned and the nitride layer has been etched down through the nitride layer and the polysilicon layer to stop on the pad oxide layer, thereby forming a nitride island and a polysilicon island over future or current active areas in the substrate that are to be protected.

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Figure 4A is a view of further processing of Figure 3A, wherein the mask has been removed and an insulation film has been deposited over the nitride island.

Figure 4B illustrates further processing of the structure in Figure 3B, wherein the mask has been removed and an insulation film has been deposited over the nitride island and the polysilicon island.

Figures 5A and 5B illustrate further processing of the structure depicted, respectively, in Figures 4A and 4B, in which the insulation film has been etched to form a spacer, a simultaneous or serial etch has formed an isolation trench, thermal oxidation or deposition within the isolation trench has formed an insulation liner therein, and wherein an optional ion implantation has formed a doped region at the bottom of the isolation trench.

Figures 6A and 6B illustrate further processing of the structure depicted, respectively, in Figures 5A and 5B, in which an isolation film has been deposited over the spacer, the isolation trench within the isolation trench liner, and the nitride island.

Figures 7A and 7B illustrate further processing of the structure depicted, respectively, in Figures 6A and 6B, wherein a planarization process has formed a first upper surface made up of the nitride island, the spacer, and the isolation film, all being substantially co-planar on the first upper surface.

Figure 8A illustrates further processing of the structure depicted in Figures 7A or 9A, wherein the semiconductor substrate has been implanted with ions, and wherein the isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have fused to form a unitary isolation structure.

Figure 8B illustrates optional further processing of the structure depicted in Figure 6B, wherein an etching process using an etch recipe that is slightly selective to oxide over nitride, has etched back the isolation film, the nitride island, and the spacer to expose the polysilicon island, and has formed a filled isolation trench which, when viewed in a

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direction that is substantially orthogonal to the cross section of the depicted word line, has the shape of a nail.

Figure 9A illustrates optional further processing of the structure depicted in Figure 6A or in Figure 7A, wherein an etch-selective recipe that is slightly selective to oxide over nitride has formed a filled isolation trench which, when viewed in cross section, has the shape of a nail.

Figure 9B illustrates further processing of the structure depicted in either Figures 7B or 8B wherein the semiconductor substrate has been implanted with ions, and wherein the isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have been fused to form a filled isolation trench.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to a method for forming a self-aligned isolation trench. The isolation trench is preferably a shallow trench isolation region that is self-aligned to an underlying active area. Stated otherwise, the inventive method forms a Narrow self-aligned Active area Isolation region that is inherently Level (NAIL). In the method of the present invention, a spacer etch and an isolation trench etch can be accomplished essentially within the same processing step.

Another aspect of the present invention relates to a combined nitride and oxide etch that is selective to polysilicon, and in which selectivity of the etch between nitride and oxide materials favors one or the other by a factor of about one half. A still further aspect of the present invention relates to the use of a polysilicon film as an etch stop or planarization marker film. The structure achieved by the method of the present invention achieves particular advantages that overcome problems of the prior art.

A starting structure for an example of a first embodiment of the present invention is illustrated in Figure 2A. In Figure 2A, a pad oxide 14 is grown upon a semiconductor substrate 12 on a semiconductor structure 10. Semiconductor substrate 12 can be substantially composed of silicon. Following growth of pad oxide 14, a nitride layer 16 is deposited over semiconductor substrate 12. Figure 2A illustrates deposition of nitride layer 16 upon pad oxide 14.

Figure 3A illustrates a step in the formation of an isolation trench by the method of the present invention. Nitride layer 16 is patterned with a mask 20. An anisotropic etch selectively removes portions of nitride layer 16. Figure 3A illustrates the result of etching with the use of mask 20, wherein nitride layer 16 has formed an insulator island 22, as seen in Figure 4A. Insulator island 22 is patterned over and protects future or current active areas (not pictured) in semiconductor substrate 12 during isolation trench processing. Following etch of nitride layer 16, mask 20 is removed.

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Figure 4A illustrates further processing of the structure depicted in Figure 3A, wherein an insulation film 26 has been deposited upon insulator island 22 and exposed portions of pad oxide 14. Insulation film 26 can be an oxide such as silicon dioxide, and can be formed for example by decomposition of tetraethyl ortho silicate (TEOS). Insulation film 26 may also be formed by a plasma enhanced chemical vapor deposition (PECVD) process so as to deposit a nitride layer such as Si_3N_4 or equivalent. When insulation film 26 is a nitride layer, insulator island 22 would be selected to be composed of a substantially different material, such as an oxide. Formation of substantially different materials between insulator island 22 and insulation film 26 facilitate selective etchback or selective mechanical planarization such as chemical-mechanical polishing (CMP) in the inventive method of forming an isolation trench.

Following deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out. The spacer etch and the isolation trench etch can be carried out with a single etch recipe that is selective to insulation film 26. Alternatively, the spacer etch and the isolation trench etch can be carried out with two etch recipes. As such, the first etch etches insulation film 26 in a spacer etch that forms a spacer 28 seen in Figure 5A. The second etch, or isolation trench etch, has an etch recipe that is selective to spacer 28 and insulator island 22, and anisotropically etches an isolation trench 32 having a side wall 50 in semiconductor substrate 12.

Spacer 28 may facet during the spacer etch such that a substantially linear spacer profile is achieved. Spacer 28 adds the advantage to the inventive process of extending the lateral dimension of the active area that is to be formed within semiconductor substrate 12 immediately beneath insulator island 22. Because spacer 28 takes up lateral space that would otherwise be available for isolation trench 32, isolation trench 32 is made narrower and the active area that is to be formed within semiconductor substrate 12 is made wider.

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Following the formation of isolation trench 32, sidewall 50 of isolation trench 32 has optionally formed thereon an insulation liner 30. For example, thermal oxidation of sidewall 50 will form insulation liner 30 within isolation trench 32. Insulation liner 30 will preferably be substantially composed of silicon dioxide. In Figure 5A it can be seen that, following thermal oxidation of sidewall 50 to form insulation liner 30 within isolation trench 32, semiconductor substrate 12 forms a rounded edge at the top of isolation trench 32. Rounding of the top of semiconductor substrate 12 at the corners of isolation trench 32 provides an added advantage of further isolating semiconductor substrate 12 immediately beneath insulator island 22; thereby an active area that will form in semiconductor substrate 12 immediately under insulator island 22 will be further isolated. The feature of rounding of the corners of semiconductor substrate 12 at the tops of isolation trenches 32 as depicted in Figures 5A and 5B is presupposed in all embodiments of the present invention as a preferred alternative.

Another method of forming insulation liner 30 is CVD of a dielectric material, or a dielectric material precursor that deposits preferentially upon sidewall 50 of isolation trench 32. The material of which insulation liner 30 is substantially composed may be particularly resistant to further etching, cleaning, or other processing conditions.

Insulation liner 30 may be substantially composed of a nitride such as Si_3N_4, or an equivalent, and can be selectively formed upon sidewall 50 of isolation trench 32. When semiconductor substrate 12 immediately adjacent to isolation trench 32 is a doped monocrystalline silicon that forms, for example, an active area for a transistor source/drain region, oxidation is avoided therein by insulation liner 30. Insulation liner is preferably substantially composed of Si_3N_4 or a non-stoichiometric variant which seals sidewall 50 so as to prevent encroachment of oxide into semiconductor substrate 12.

Following formation of insulation liner 30, ion implantation is optionally carried out to form a doped trench bottom 34 at the bottom of isolation trench 32. For example, if

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semiconductor wafer 10 comprises an N-doped silicon substrate, implantation of P-doping materials at the bottom of isolation trench 32 will form a P-doped trench bottom 34. Ion implantation may be carried out in a field implantation mode. If a complementary metal oxide semiconductor (CMOS) is being fabricated, however, masking of complimentary regions of semiconductor substrate 12 is required in order to achieve the differential doping thereof. For an N-doped silicon substrate, a high breakdown voltage may be achieved by P-doping. A low breakdown voltage may achieved by N-doping, and an intermediate breakdown voltage may be achieved by no doping. Because the present invention relates to formation of isolation trenches, P-doping in an N-well region, or N-doping in a P-well region are preferred.

Preferably, implantation of P-doping ions is carried out to form doped trench bottom 34 in a direction that is substantially orthogonal to the plane of pad oxide 14. Slightly angled implantation of P-implantation ions may be carried out to enrich or broaden the occurrence of P-doping ions in doped trench bottom 34 at the bottom of isolation trench 32. If P-doping is carried out where semiconductor substrate 12 is N-doped, care must be taken not to dope through insulation liner 30 on sidewall 50 near pad oxide 14, which may cause detrimental deactivation of active areas (not shown) in semiconductor substrate 12.

Following optional implantation of doping ions, it may be desirable, depending upon the intended shape and design of the isolation trench, to remove all or a portion of spacer 28. The isolation trench formed by the inventive method, however, will preferably include at least a portion of spacer 28 that extends away from the isolation trench 32.

As seen in Figure 6A, isolation trench 32 is filled by an isolation film 36 which also is formed upon insulator island 22. Isolation film 36 can formed by a deposition process using, for example, TEOS as a precursor.

An optional processing step of the inventive method is to fuse together spacer 28, pad oxide 14, and isolation film 36. The processing technique for such fusion is preferably a heat

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treatment of semiconductor structure 10. If such fusion is contemplated, it is also desirable that spacer 28, pad oxide 14, and isolation film 36 all be composed of substantially the same material, as fusion is best facilitated with common materials.

It is preferable, at some point in fabrication of the isolation trench, to densify the fill material of the isolation trench. Densification is desirable because it helps to prevent separation of materials in contact with the fill material. As seen in Figure 6A, densification will prevent isolation film 36 from separating at interfaces with spacer 28, pad oxide layer 14, and insulation liner 30. It is preferable to perform densification of isolation film 36 immediately following its deposition. Depending upon the specific application, however, densification may be carried out at other stages of the process. For example, densification of isolation film 36 by rapid thermal processing (RTP) may make either etchback or CMP more difficult. As such, it is preferable to densify later in the fabrication process, such as after planarizing or etchback processing.

Figure 7A illustrates a subsequent step of formation of the isolation trench wherein insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process. Preferably, planarization will be selective to isolation film 36, and relatively slightly selective to insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to be slightly selective to spacer 28 over insulator island 22. Preferably spacer 28 and isolation film 36 are made from the same material such that the etch will be substantially uniform as to the selectivity thereof with respect to spacer 28 and isolation film 36 over insulator island 22.

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First upper surface 38 is illustrated as being substantially planar in Figure 7A. It will be appreciated by one of ordinary skill in the art that first upper surface 38 will form a nonplanar profile or topography depending upon the selectivity of the etch recipe or of the chemical used in a planarization technique such as CMP. For example, where reduced island 52 is formed from a nitride material and isolation film 36 is formed from an oxide material, first upper surface 38 would undulate as viewed in cross section with more prominent structures being the result of an etch or planarization technique more selective thereto.

In Figure 7A, reduced island 52 has been formed from insulator island 22. Additionally, portions of isolation film 36 and spacer 28 remain after planarization. Reduced island 52 preferably acts as a partial etch stop.

Figure 8A illustrates the results of removal of reduced island 52. Reduced island 52 is preferably removed with an etch that is selective to isolation film 36 and spacer 28, leaving an isolation structure 48 that extends into and above isolation trench 32, forming a nail shaped structure having a head 54 extending above and away from isolation trench 32 upon an oxide layer 44. The future or current active area of semiconductor substrate 12, which may be at least partially covered over by head 54, is substantially prevented from a detrimental charge and current leakage by head 54.

Phantom lines 60 in Figure 8A illustrate remnants of pad oxide layer 14, insulation liner 30, and spacer 28 as they are optionally thermally fused with isolation film 36 to form isolation structure 48. Isolation structure 48, illustrated in Figure 8A, comprises a trench portion and a flange portion which together, when viewed in cross section, form the shape of a nail.

The trench portion of isolation structure 48 is substantially composed of portions of isolation film 36 and insulation liner 30. The trench portion intersects the flange portion at a second upper surface 40 of semiconductor substrate 12 as seen in Figure 8A. The trench portion also has two sidewalls 50. Figure 8A shows that the trench portion is substantially

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parallel to a third upper surface 42 and sidewalls 50. The flange portion is integral with the trench portion and is substantially composed of portions of pad oxide layer 14, spacer 28, and isolation film 36. The flange portion has a lowest region at second upper surface 40 where the flange portion intersects the trench portion. The flange portion extends above second upper surface 40 to third upper surface 42 seen in Figure 8A. Upper surfaces 40, 42 are substantially orthogonal to two flange sidewalls 64 and sidewall 50. The flange portion is substantially orthogonal in orientation to the trench portion. The flange portion may also include a gate oxide layer 44 after gate oxide layer 44 is grown.

Following formation of isolation structure 48, it is often useful to remove pad oxide 14, seen in Figure 8A, due to contamination thereof during fabrication of isolation structure 48. Pad oxide 14 can become contaminated when it is used as an etch stop for removal of reduced island 52. For example, pad oxide 14 may be removed by using aqueous HF to expose second upper surface 40. A new oxide layer, gate oxide layer 44, may then be formed on second upper surface 40 having third upper surface 42.

Semiconductor structure 10 may be implanted with ions as illustrated by arrows seen in Figure 8A. This implantation, done with N-doping materials in an N-well region, for example, is to enhance the electron conductivity of the active area (not shown) of semiconductor substrate 12. Either preceding or following removal of pad oxide 14 seen in Figure 8A, an enhancement implantation into the active area of semiconductor substrate 12 may be carried out, whereby preferred doping ions are implanted on either side of isolation structure 48.

Ion implantation into semiconductor substrate 12 to form active areas, when carried out with isolation structure 48 in place, will cause an ion implantation concentration gradient to form in the region of semiconductor substrate 12 proximate to and including second upper surface 40. The gradient will form within semiconductor substrate 12 near second upper surface 40 and immediately beneath the flange sidewalls 64 as the flange portion of isolation

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structure 48 will partially shield semiconductor substrate 12 immediately therebeneath. Thus, an ion implant gradient will form and can be controlled in part by the portion of semiconductor substrate 12 that is covered by head 54.

Gate oxide layer 44 is formed upon second upper surface 40 after pad oxide 14 has been removed to form portions of third upper surface 42. The entirety of third upper surface 42 includes head 54 of isolation structure 48 as it extends above gate oxide layer 44 and gate oxide layer 44.

In a variation of the first embodiment of the present invention, the structure illustrated in Figure 6A is planarized by use of a single etchback process. The single etchback uses an etch recipe that has a different selectivity for insulator island 22 than for isolation film 36. In this alternative embodiment, spacer 28, dielectric film 36, and pad oxide 14 are composed of substantially the same material. Insulator island 22 has a composition different from that of isolation film 36. For example, isolation film 36 and spacer 28 are composed of SiO_2, and insulator island 22 is composed of silicon nitride.

The etch recipe for the single etchback is chosen to be selective to isolation film 36 such that, as upper surface 58 of isolation film 36 recedes toward pad oxide 14 and eventually exposes insulator island 22 and spacer 28, insulator island 22 has a greater material removal rate than spacer 28 or isolation film 36. As such, a final isolation structure 48 illustrated in Figure 9A is achieved. Pad oxide 14 acts as an etch stop for this etch recipe. A residual depression of isolation film 36 may appear centered over filled isolation trench 32. A depression would be created, centered above isolation trench 32, during the filling of isolation trench 32 with isolation film 36, as seen in Figure 6A. Where a depression is not detrimental to the final isolation structure 48 as illustrated in Figure 9A, this selective etch recipe alternative may be used.

Semiconductor structure 10, as illustrated in Figure 9A, can be seen to have a substantially continuous isolation structure substantially covering semiconductor

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substrate 12. An upper surface 42a of isolation structure 48 includes the head portion or nail head 54. Semiconductor substrate 12 is covered at an upper surface 42b by either a pad oxide layer or a gate oxide layer. Another upper surface 42c comprises the upper surface of the pad oxide layer or gate oxide layer.

A starting structure for an example of a second embodiment of the present invention is illustrated in Figure 2B. In Figure 2B, pad oxide layer 14 is grown upon semiconductor substrate 12 and a polysilicon layer 18 is deposited upon pad oxide layer 14. This embodiment of the present invention parallels the processing steps of the first embodiment with the additional processing that takes into account the use of polysilicon layer 18.

Figure 3B illustrates etching through nitride layer 16 and polysilicon layer 18 to stop on pad oxide layer 14. The etch creates both an insulator island 22 and a polysilicon island 24 formed, respectively, from nitride layer 16 and polysilicon layer 18.

Figure 4B illustrates further processing of the structure depicted in Figure 3B, wherein insulation film 26 has been deposited upon insulator island 22, laterally exposed portions of polysilicon island 24, and exposed portions of pad oxide layer 14. Following deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out similarly to the spacer etch and isolation trench etch carried out upon semiconductor structure 10 illustrated in Figure 5A.

Figure 5B illustrates the results of both the spacer etch and the isolation trench etch and optional implantation of isolation trench 32 to form doped well 34 analogous to doped trench bottom 34 illustrated in Figure 5A. Formation of insulation liner 30 within isolation trench 32 preferentially precedes implantation to form doped trench bottom 34. Following optional implantation of doping ions, full or partial removal of spacer 28 may optionally be performed as set forth above with respect to the first embodiment of the invention.

Figure 6B illustrates a subsequent step in fabrication of an isolation trench according to the second embodiment of the inventive method, wherein isolation film 36 is deposited

both within isolation trench 32, and over both of insulator island 22 and spacer 28. As set forth above, densification of isolation film 36 is a preferred step to be carried out either at this stage of fabrication or at a subsequent selective stage. Planarization or etchback of isolation film 36 is next carried out as set forth in the first embodiment of the present invention, and as illustrated in Figure 7B.

The process of planarization or etchback of isolation film 36 reduces insulator island 22 to form reduced island 52 as illustrated in Figure 7B. Next, additional selective ion implantations can be made through polysilicon island 24 and into the active area of semiconductor substrate 12 that lies beneath polysilicon island 24.

In Figure 8B, it can be seen in phantom that spacer 28 has a top surface that is co-planar with third upper surface 42 of isolation structure 48 after planarization. Polysilicon island 24 and spacer 28 are formed as shown in Figure 8B. Removal of spacer 28 from the structures illustrated in Figure 8B can be accomplished by patterning and etching with a mask that covers head 54 that extends above and away from isolation trench 32 seen in Figure 8B. The etching process exposes a surface on semiconductor substrate 12 upon which a gate oxide layer is deposited or grown.

To form the structure seen in Figure 9B, semiconductor structures 10 of Figures 7B or 8B are subjected to implantation of semiconductor substrate 12 with ions. Semiconductor structure 10 is then subjected to a heat treatment so as to fuse together isolation film 36, optional pad oxide layer 14, insulation liner 60, and spacer 28 into an integral filled isolation trench.

Subsequent to the process illustrated in Figures 6A-8A and 6B-9B a final thermal treatment, or subsequent thermal treatments, can be performed. Heat treatment may cause isolation structure 48 to be wider proximal to upper surface 42 than proximal to doped trench bottom 34. When so shaped, an unoxidized portion of the active area of semiconductor substrate 12 that forms sidewall 50 would have a trapezoidal shape when viewed in cross

section, where the widest portion is upper surface 40 and the narrowest portion is at doped trench bottom 34. Where a trapezoidal shape of the trench portion causes unwanted encroachment into the active area of semiconductor substrate 12, the optional formation of insulation liner 30 from a nitride material or equivalent is used to act as an oxidation barrier for sidewall 50. Semiconductor structure 10 is illustrated in Figure 9B as being implanted by doping ions, as depicted with downwardly-directed arrows. Following a preferred implantation, thermal processing may be carried out in order to achieve dopant diffusion near upper surface 42b of implanted ions residing within semiconductor substrate 12. Due to head 54 extending onto semiconductor substrate 12, a doping concentration gradient can be seen between the active area 53a and the active area 53b. The starting and stopping point of the doping concentration gradient in relation to flange sidewalls 64 will depend upon the duration and temperature of a thermal treatment.

The present invention may be carried out wherein spacer 28 and isolation film 36 are substantially composed of the same oxide material, and insulator island 22 is substantially composes of a nitride composition. Other compositions may be chosen wherein etch selectivity or CMP selectivity slightly favors insulator island 22 over both spacer 28 and isolation film 36. The specific selection of materials will depend upon the application during fabrication of the desired isolation trench.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is:

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1. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

2. A method according to Claim 1, further comprising forming a liner upon a sidewall of each said isolation trench.

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3. A method according to Claim 2, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

4. A method according to Claim 2, wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.

5. A method according to Claim 1, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

6. A method according to Claim 1, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

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7. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein:

material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said pad oxide layer; and

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said first dielectric layer is in contact with at least a pair of said spacers and said pad oxide layer.

8. A method according to Claim 7, further comprising:

removing said pad oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

9. A method according to Claim 7, wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from of about 1:1 to about 2:1.

10. A method according to Claim 9, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

11. A method according to Claim 7, wherein said upper surface for each said isolation trench is formed by the steps comprising:

chemical mechanical planarization, wherein said conformal layer, said spacers, and said first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, said second upper surface being situated above said pad oxide layer.

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12. A method according to Claim 11, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

13. A method according to Claim 11, wherein said ratio in a range from about 1.3:1 to about 1.7:1.

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14. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding electrically active region below the termination of said each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a second silicon dioxide layer, said second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers; and

selectively removing said second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein material that

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is electrically insulative extends continuously between and within said plurality of isolation trenches.

15. A method according to Claim 14, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

16. A method according to Claim 14, wherein said liner is composed of silicon nitride.

17. A method according to Claim 15, further comprising:

removing said oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

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18. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces

further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces.

19. A method according to Claim 18, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

20. A method according to Claim 18, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

21. A method according to Claim 18 , further comprising, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench that extends from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and wherein said conformal third layer is composed of an electrically conductive material.

22. A method according to Claim 21, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

23. A method according to Claim 21, wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter.

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24. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein said upper surface for each said isolation trench is formed from said conformal third layer, said spacers, and said first dielectric layer.

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25. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

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forming a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

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26. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer by an etch using an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

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27. A method according to Claim 26, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

28. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

chemical mechanical planarization of said conformal third layer, said spacers, and said first dielectric layer to form a planar first upper surface; and

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an etch that forms a planar second upper surface, said second upper surface being situated above said oxide layer;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

29. A method according to Claim 28, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

30. A method of forming and filling an isolation trench according to Claim 28, wherein said ratio in a range from about 1.3:1 to about 1.7:1.

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31. A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers; and

planarizing said second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

32. A method according to Claim 31, wherein each said liner is a thermally grown oxide of said semiconductor substrate, and wherein said second layer is composed on an electrically conductive material.

33. A method according to Claim 31, wherein each said liner is composed of silicon nitride, and wherein said second layer is composed on an electrically conductive material.

34. A method according to Claim 31, further comprising:

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate; and

forming a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and

selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

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35. A method for a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said

isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer.

36. The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each said isolation trench.

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37. The method as defined in Claim 36, wherein the doped trench bottom has a width, each said the isolation trench has a width, and the width of each said doped trench bottom is greater than the width of the respective isolation trench.

38. A method for a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said

isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer.

39. The method as defined in Claim 38, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of said isolation trenches.

40. The method as defined in Claim 39, wherein:

the doped trench bottom has a width;

each said isolation trench has a width; and

the width of each said doped trench bottom is greater than the width of the respective isolation trench.

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41. A method of a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface;

forming first and second isolation trenches each:

extending into and being defined by the semiconductor substrate;

having an opening thereto at the top surface of the semiconductor substrate; and

extending below and being centered between a pair of spacers situated above the top surface of the semiconductor substrate;

and wherein:

an electrically insulative material extends continuously between and within the first and second isolation trenches; and

a planar surface begins at the first isolation trench and extends continuously to the second isolation trench.

42. A method for a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate

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adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

forming a planar upper surface from said second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer.

43. A method of a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said

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first spacer of said second isolation structure is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

forming a planar upper surface formed from said second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer.

ABSTRACT OF THE INVENTION

The present invention relates to a method for forming an isolation trench structure in a semiconductor substrate without causing deleterious topographical depressions in the upper surface thereof which cause current and charge leakage to an adjacent active area. The inventive method forms a pad oxide upon a semiconductor substrate, and then forms a nitride layer on the pad oxide. The nitride layer is patterned with a mask and etched to expose a portion of the pad oxide layer and to protect an active area in the semiconductor substrate that remains covered with the nitride layer. A second dielectric layer is formed substantially conformably over the pad oxide layer and the remaining portions of the first dielectric layer. A spacer etch is then carried out to form a spacer from the second dielectric layer. The spacer is in contact with the remaining portion of the first dielectric layer. An isolation trench etch follows the spacer etch. An optional thermal oxidation of the surfaces in the isolation trench may be performed, which may optionally be followed by doping of the bottom of the isolation trench to further isolate neighboring active regions on either side of the isolation trench. A conformal layer is formed substantially conformably over the spacer, over the remaining portions of the first dielectric layer, and substantially filling the isolation trench. Planarization of the conformal layer follows, either by CMP or by etchback or by a combination thereof. An isolation trench filled with a structure results. The resulting structure has a flange and shaft, the cross section of which has a nail shape in cross section.

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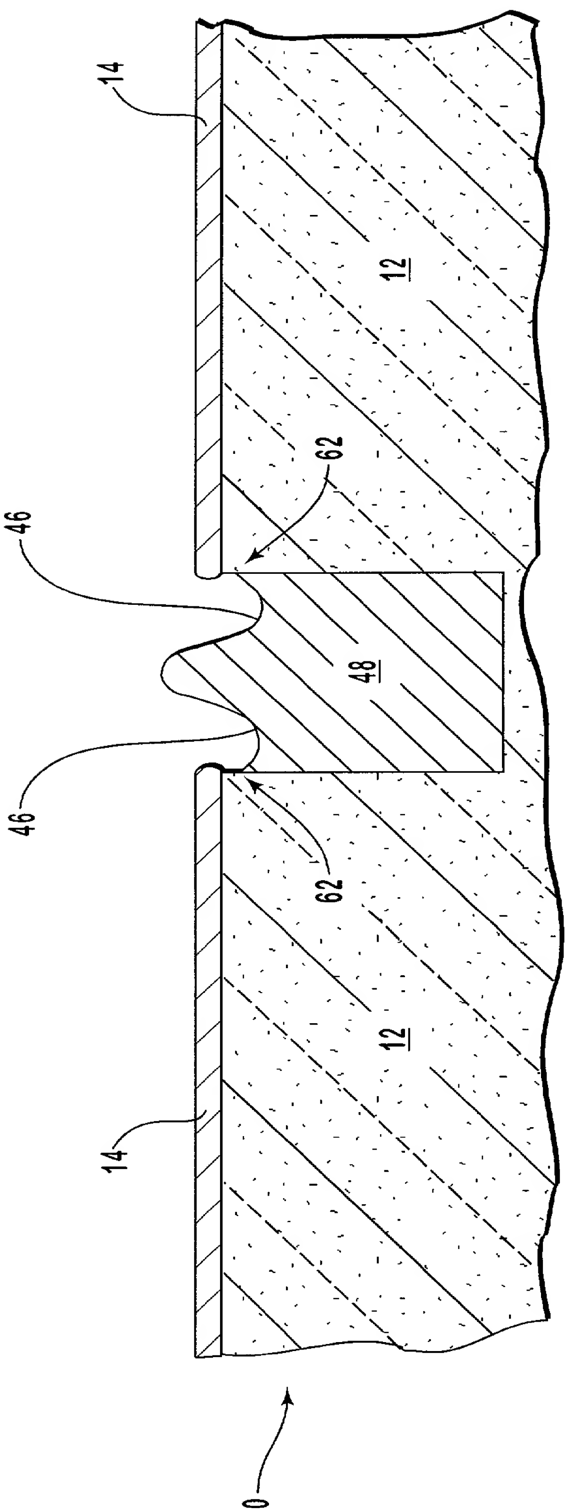

FIG. 1
(PRIOR ART)

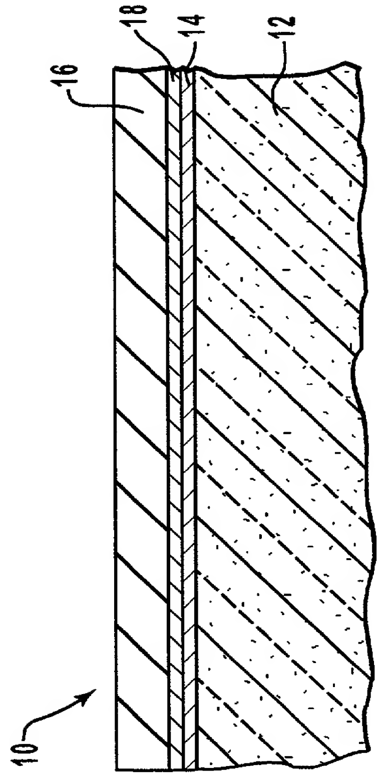

FIG. 2B

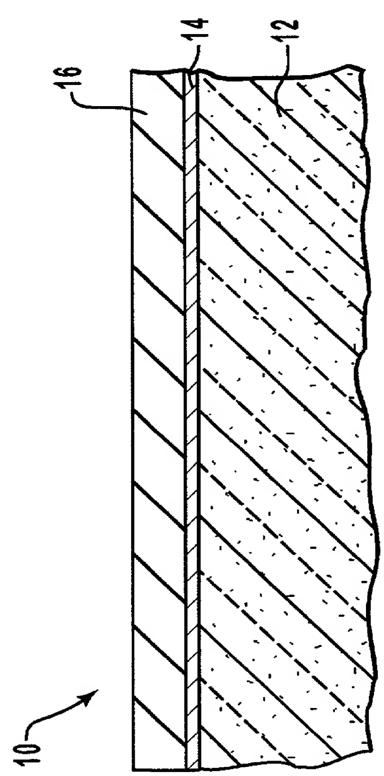

FIG. 2A

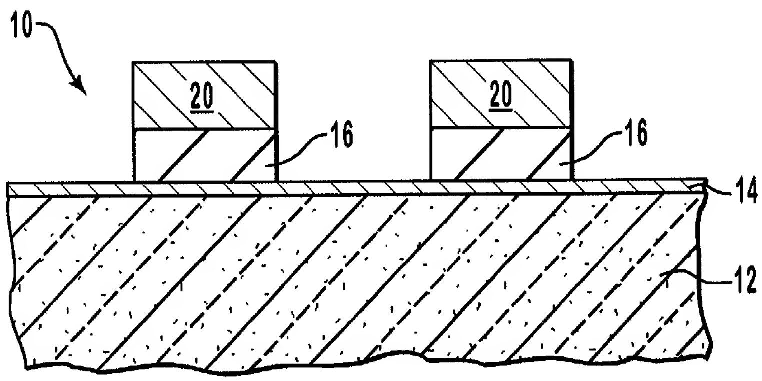

FIG. 3A

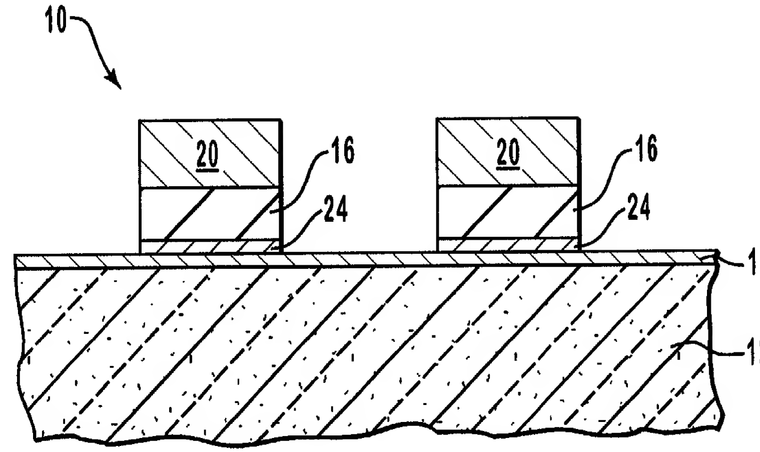

FIG. 3B

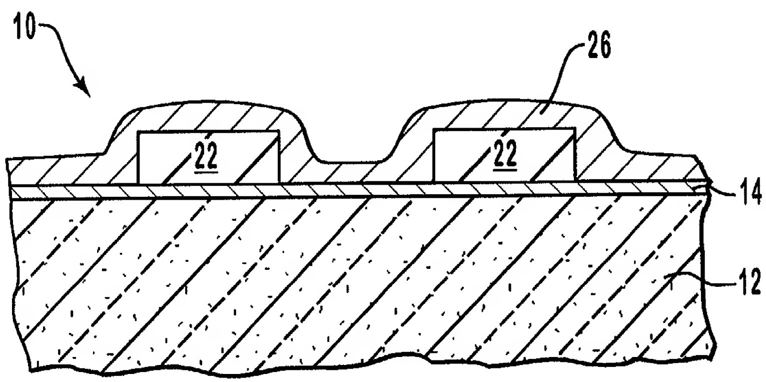

FIG. 4A

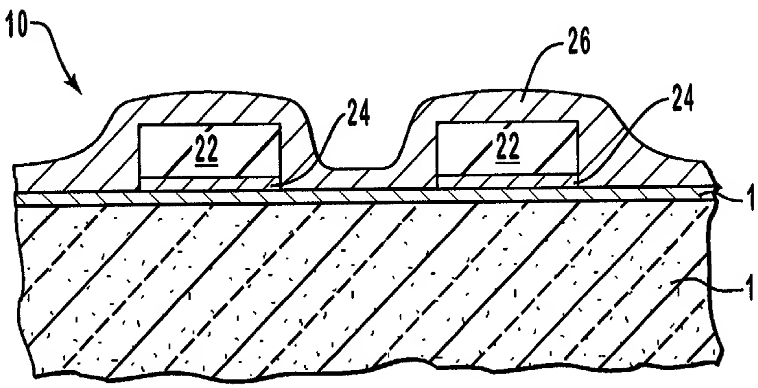

FIG. 4B

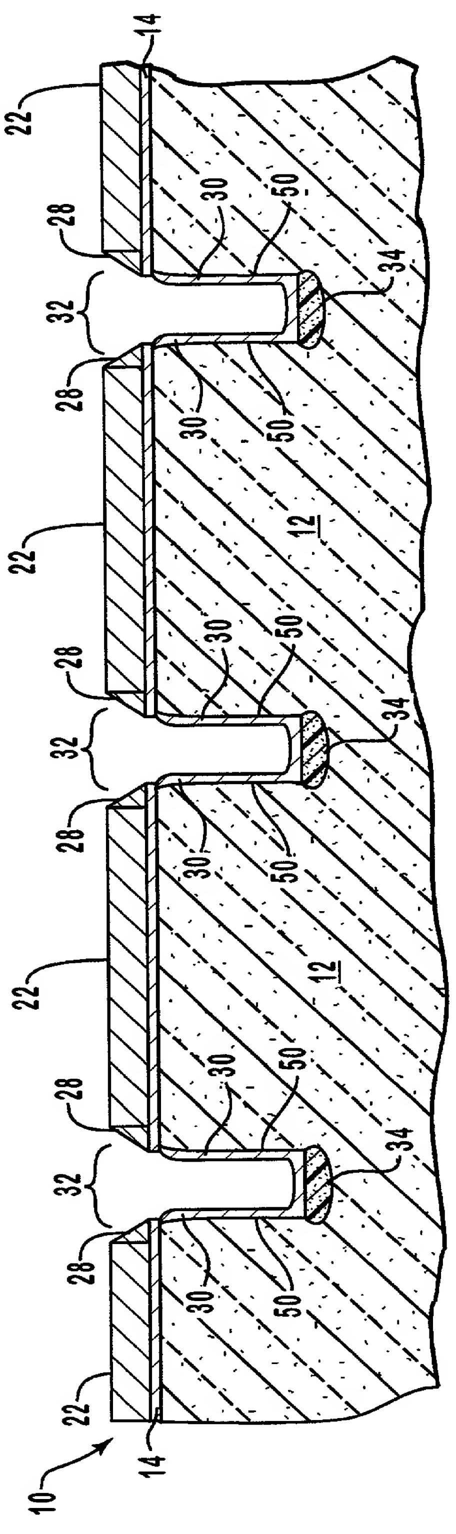

FIG. 5A

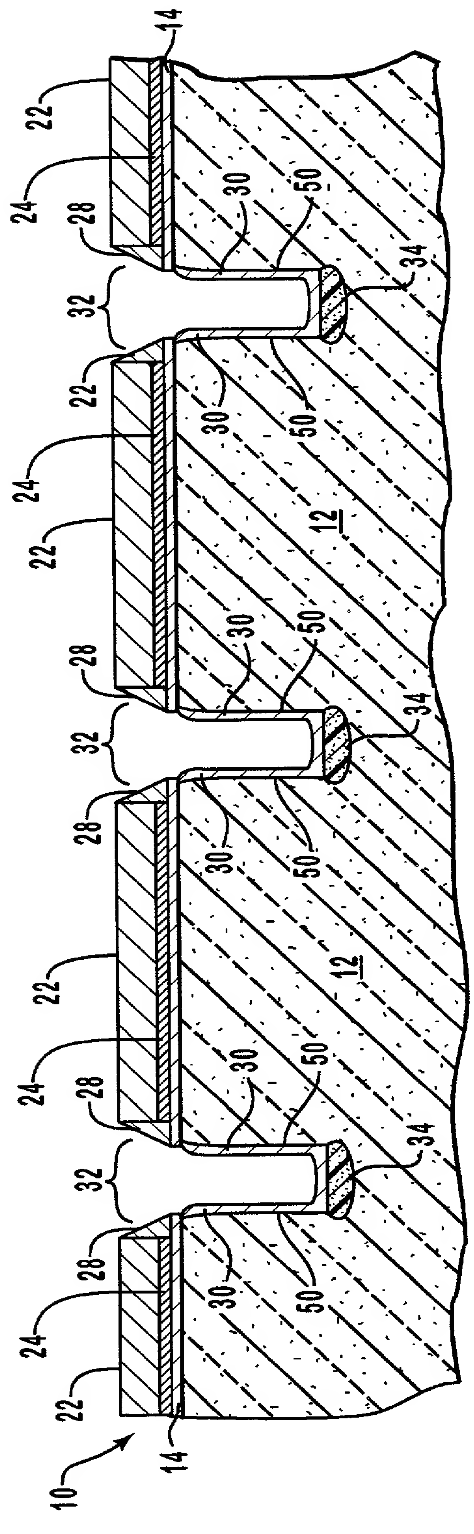

FIG. 5B

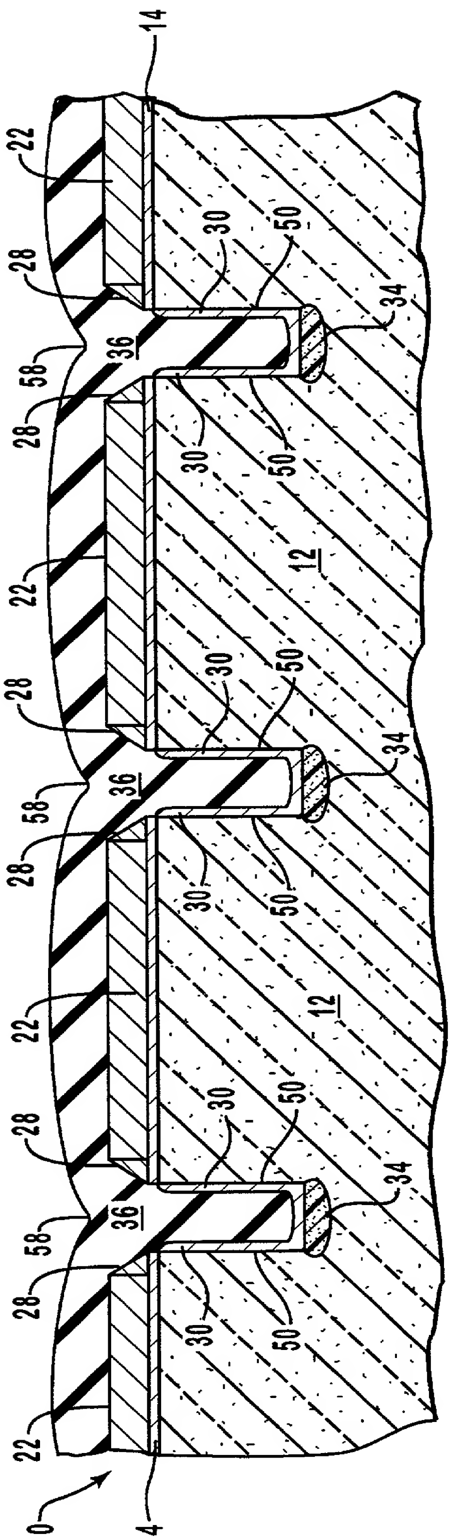

FIG. 6A

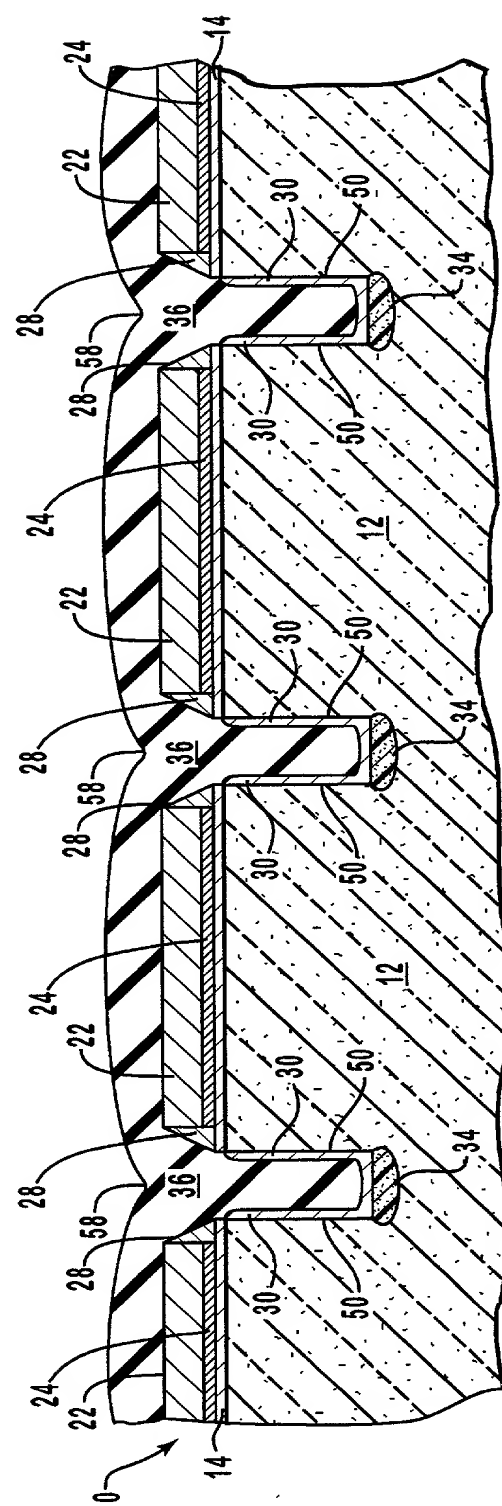

FIG. 6B

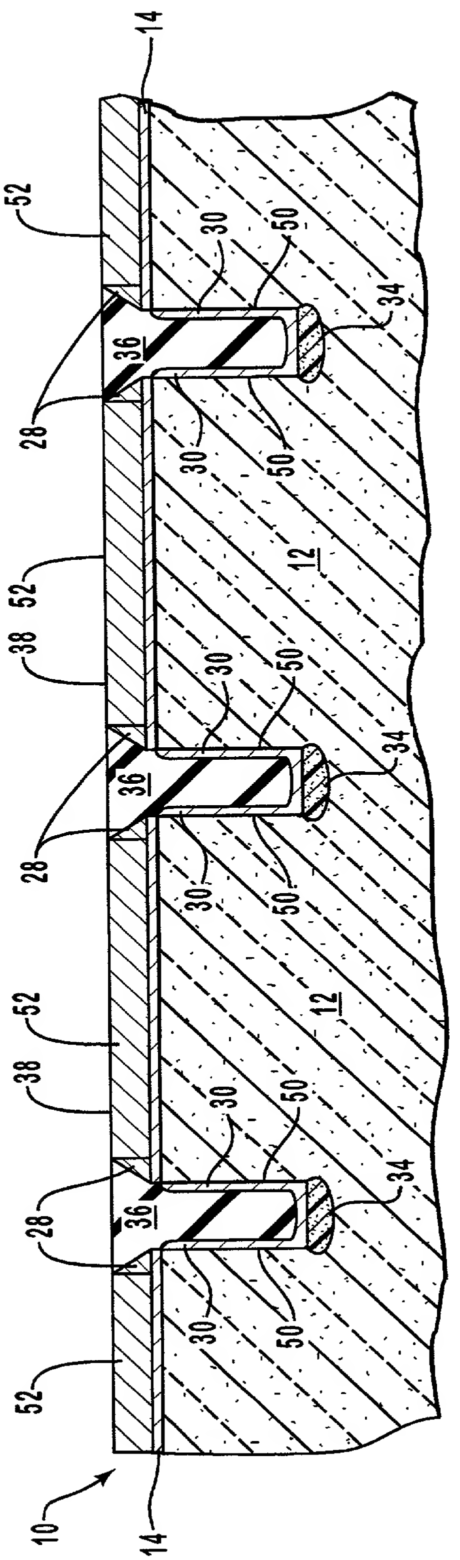

FIG. 7A

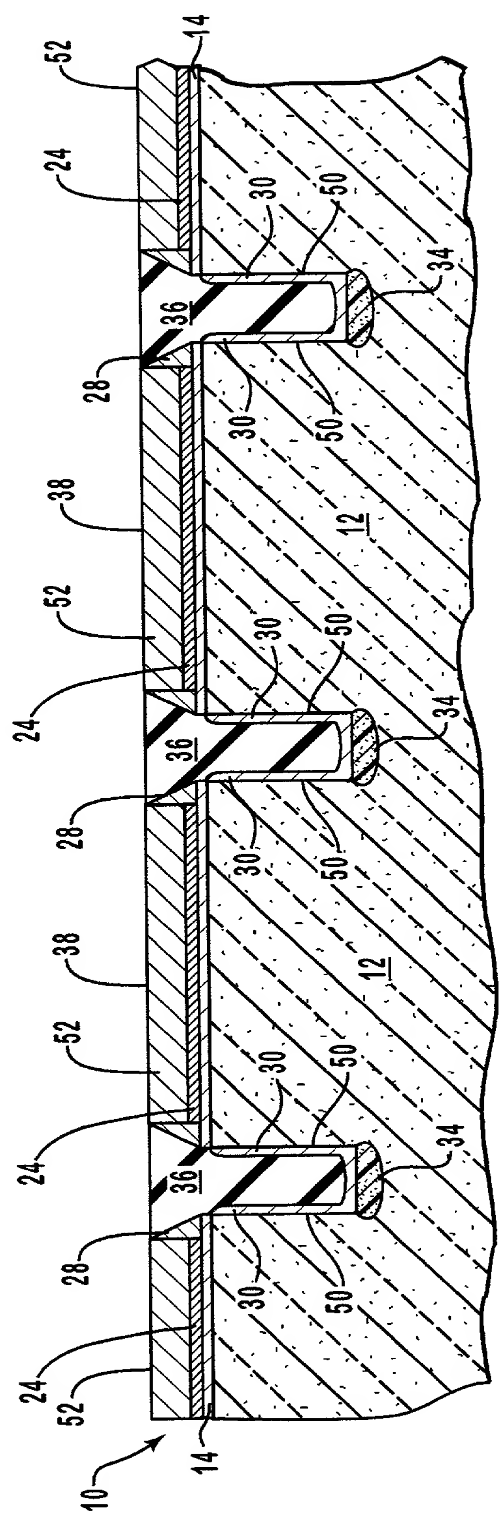

FIG. 7B

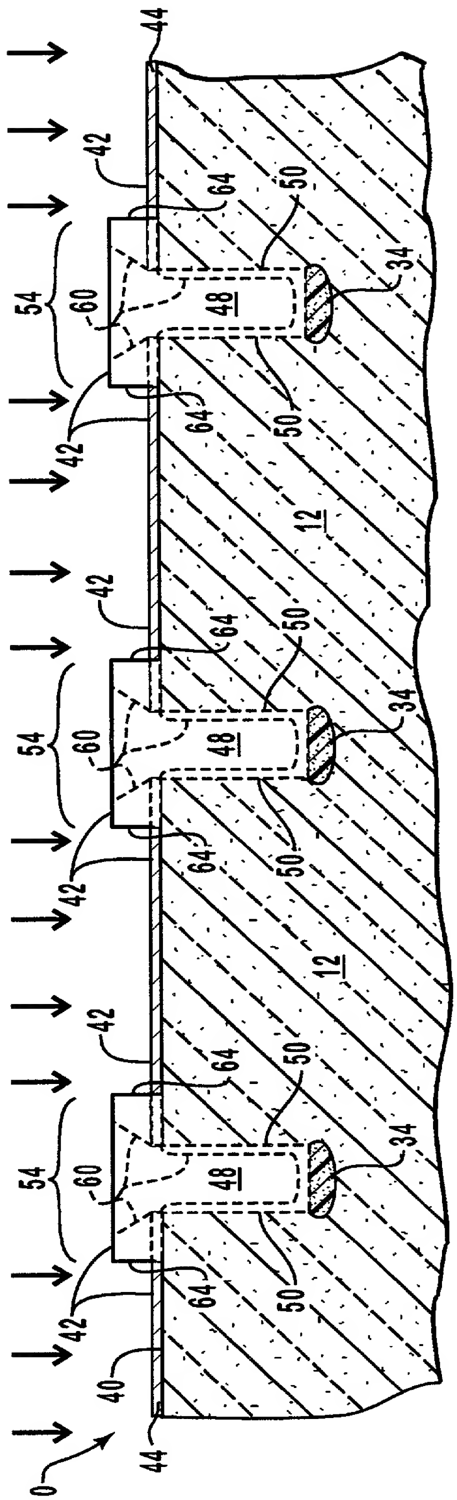

FIG. 8A

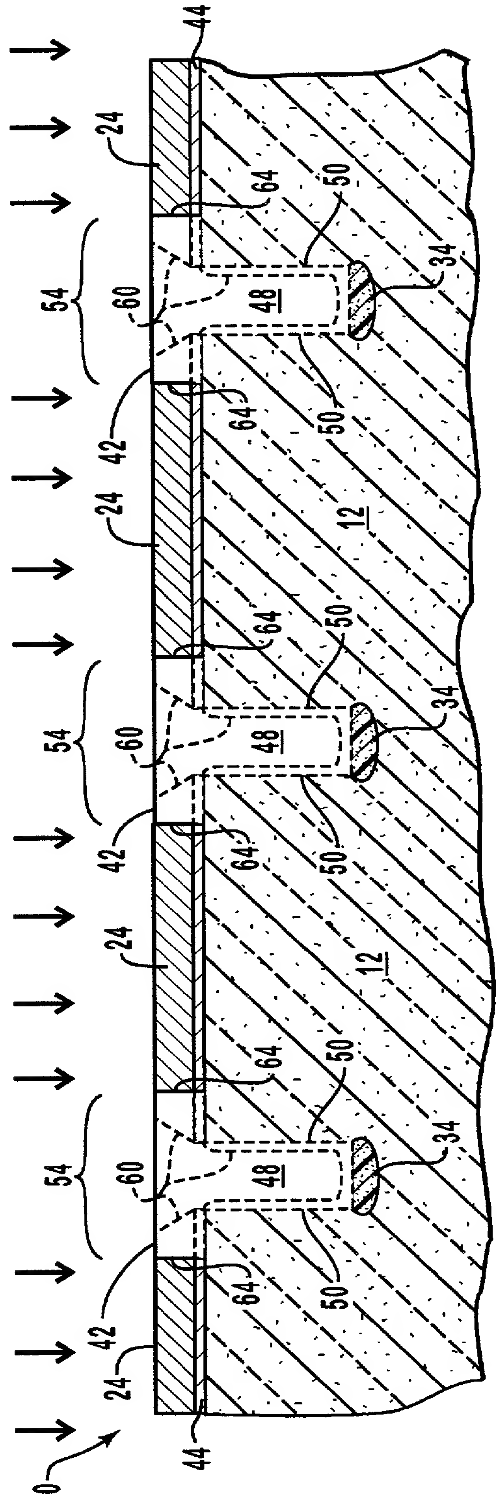

FIG. 8B

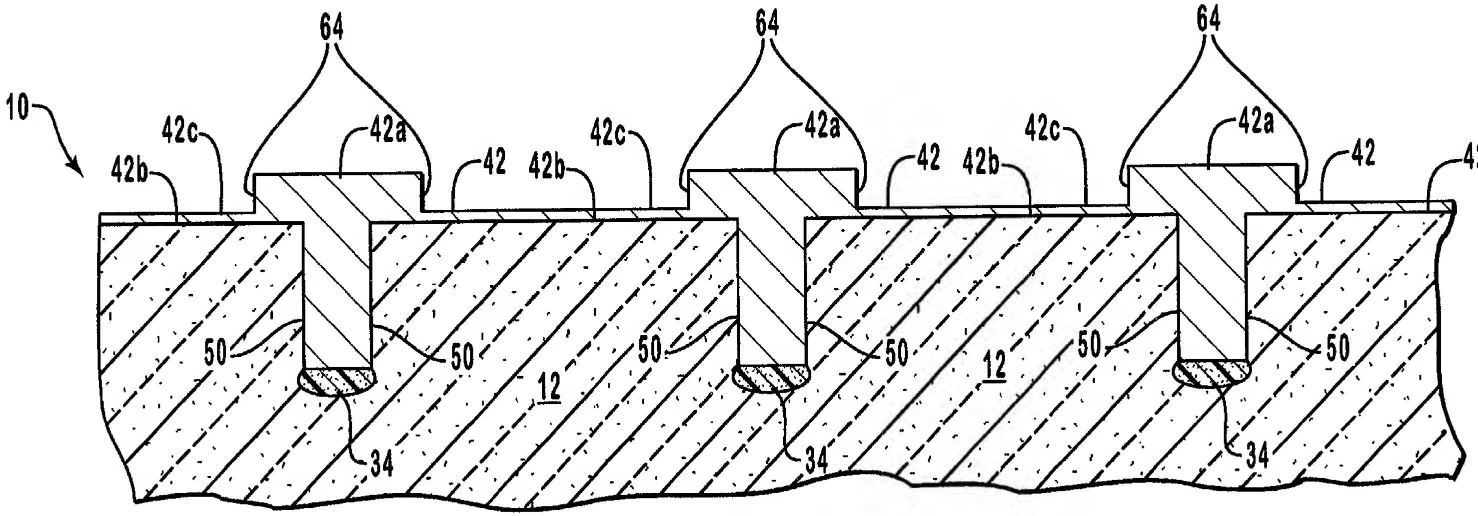
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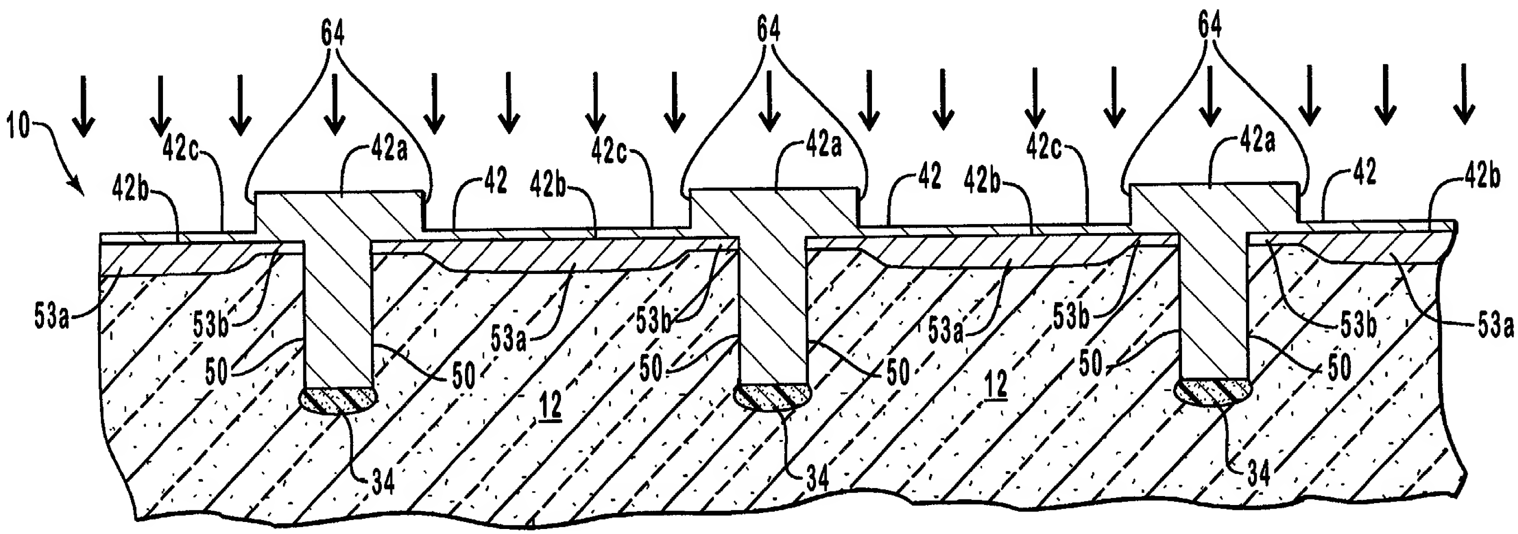
FIG. 9A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53a
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53b
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53b
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53a
34

FIG. 9B

DECLARATION, POWER OF ATTORNEY, AND PETITION

We, Fernando Gonzalez, David Chapek and Randhir P. S. Thakur, declare: that we are citizens of United States of America, United States of America, and India, respectively; that our residences and post office addresses are 2579 S. Flotilla Avenue, Boise, Idaho 83706, 3344 Gekeler Lane #M-304, Boise, Idaho 83706, and 3545 Bridgeporte Place, Boise, Idaho 83706, respectively; that we verily believe we are the original, first, and joint inventors of the subject matter of the invention or discovery entitled METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH for which a patent is sought and which is described and claimed in the specification attached hereto; that we have reviewed and understand the contents of the above-identified specification, including the claims referred to, and that we acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

We hereby appoint as our attorneys and/or patent agents: H. ROSS WORKMAN, Registration No. 25,230; RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; JONATHAN W. RICHARDS, Registration No. 29,843; JOHN C.

STRINGHAM, Registration No. P-40,831; MICHAEL F. KRIEGER, Registration No. 35,232; BRADLEY K. DeSANDRO, Registration No. 34,521; JOHN M. GUYNN, Registration No. 36,153; GREGORY M. TAYLOR, Registration No. 34,263; DANA L. TANGREN, Registration No. 37,246; ERIC L. MASCHOFF, Registration No. 36,596; KEVIN B. LAURENCE, Registration No. 38,219; SUSAN K. MORRIS, Registration No. 39,780, JEFFREY L. RANCK, Registration No. 38,590; C. J. VEVERKA, Registration No. P-40,858; JONATHAN D. WOOD, Registration No. 39,076; ROBYN L. PHILLIPS, Registration No. 39,330; DAVID B. DELLENBACH, Registration No. 39,166; TIMOTHY M. FARRELL, Registration No. 37,321; LENA I. VINITSKAYA, Registration No. 39,448; JOHN N. GREAVES, Registration No. 40,362; KEVIN K. JOHANSON, Registration No. 38,506; MICHAEL L. LYNCH, Registration No. 30,871; and LIA P. DENNISON, Registration No. 34,095, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. All correspondence and telephonic communications should be directed to:

BRADLEY K. DeSANDRO
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Wherefore, we pray that Letters Patent be granted to us for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 18th day of March, 1997.

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Signed at Boise, ID this 18th day of March, 1997.

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Signed at Boise, Idaho this 18th day of March, 1997.

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